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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,108	02/22/2001	Thomas A. Manning	109898.125	4591

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HALE AND DORR, LLP  
60 STATE STREET  
BOSTON, MA 02109

EXAMINER
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PUENTE, EMERSON C

ART UNIT	PAPER NUMBER
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2184

DATE MAILED: 10/23/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/788,108

Applicant(s)

MANNING ET AL.

Examiner

Emerson C Puente

Art Unit

2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 22 February 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☐ Claim(s) \_\_\_\_\_ is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1, 2, 5 and 6 is/are allowed.
- 6) ☒ Claim(s) 3, 4, 7 and 8 is/are rejected.
- 7) ☒ Claim(s) 1, 3, and 7 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4. 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

Claims 1-8 have been examined.

### *Claim Objections*

Claim 1, 3, and 7 are objected to because of the following informalities:

In regards to claim 1, please change the comma to a period (see line 20 of claim).

In regards to claim 3, the phrase "the mastership resolution determination unit" lacks antecedent basis.

In regards to claim 7, please change phrase "a second signals" to "a second signal" (see line 9 of claim).

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,614,752 of Parrish et al. referred hereinafter "Parrish".

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In regards to claim 3, Parrish discloses a system for indicating and determining a master unit from a plurality of logic units, comprising:

- a first logic unit configured to output a first obey signal (see figure 1 item 12);
- a second logic unit configured to output a second obey signal, wherein the first obey signal and the second obey signal are clocked signals (see figure 1 item 12 and column 9 lines 58-65); and

- a mastership determination logic control unit coupled to the first and second obey signals, the mastership resolution determination unit configured to monitor the first and second obey signals. Parrish discloses the detection of a loss of signal or other fault associated with the "A" system clock signal (see column 10 lines 10-15), thus indicating a mastership determination logic control unit coupled to the first and second obey signals, the mastership resolution determination unit configured to monitor the first and second obey signals.

wherein the mastership determination logic unit is further configured to indicate whether the first or second logic unit is the master unit based on the first and second obey signals. Parrish discloses the switchover to the "B" system clock signal when the master clock signal "A" fails, making B the master clock signal, thus indicating the first or second logic unit is the master unit based on the first and second obey signals (see column 10 lines 10-15).

In regards to claim 7, Parrish discloses a method and determining a master unit from a plurality of logic units, comprising:

- determining that a first logic unit is the master logic unit when only a first obey signal output is time varying (see column 9 line 58 to column 10 lines 4);

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determining that a second logic unit is the master unit when only a second obey signal output is time varying. Parrish discloses if the clock master (first logic unit) has failed, it becomes isolated, thus indicating only the other controller or second logic unit is time varying, and a switchover to the "B" system clock is initiated, thus making the other switch unit controller or second logic unit the master (see column 10 lines 9-25).

determining that the first logic unit is the master unit when a first signal received by the first logic unit and a second signal received by the second logic unit are time varying in-phase. Parrish discloses a master controller and a slave controller that synchronizes its "B" frame pulses with the "A" frame pulses from the master, indicating the first logic unit is master unit when a first signal received by the first logic unit and a second signal received by the second logic unit are synchronized or time varying in-phase (see column 9 lines 15-30).

determining that the second logic unit is the master unit when the first and second signals are time varying out-of-phase. Parrish discloses in response to other faults associated with "A" system clock (which would result in loss of synchronization, thus indicating a time varying out-of-phase signal), a switchover to the "B" system clock is initiated, thus making the other switch unit controller or second logic unit the master (see column 10 lines 9-25).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parrish in view of US Patent No. 5,422,915 of Byers et al. referred hereinafter "Byers".

In regards to claim 4 and 8, Parrish discloses wherein the first and second obey signals are analyzed by the mastership determination logic unit to detect a fault when it occurs.

However Parrish fails to disclose wherein the first obey signal includes a redundant trace signal and the second obey signal includes a redundant trace signal.

Byers discloses a primary clock signal drive and a redundant clock signal drive, indicating a redundant trace signal (see figure 6 item 106,108, 110,112 and column 11 lines 25-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Parrish wherein the first obey signal includes a redundant trace signal and the second obey signal includes a redundant trace signal. A person of ordinary skill in the art would have been motivated to make the modification to Parrish because redundant clock signal drive or redundant trace signals provides clock signal which can be selected upon a failure of the primary, as per teaching of Byers (see column 11 lines 30-34).

***Allowable Subject Matter***

Claims 1-2 are objected to for reasons stated in claim objections, but would be allowed if modified to eliminate informalities disclosed in claim objections.

Claims 5-6 are allowed.

*Examiner's Statement of Reason for Allowance*

The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claims 1 and 5 are allowable over the prior art of record because the Examiner found neither prior art cited in its entirety, nor based on the prior art, found any motivation to combine any of the said prior arts.

The primary reason for allowance for claim 1 is the inclusion of logic to control a phase relationship of the second obey signal relative to the first obey signal in response to at least one of the first and second input signals in conjunction with the rest of the limitation set forth in the claim.

The primary reason for allowance for claim 5 is the inclusion of a phase relationship of the second obey signal relative to the first obey signal is controllable by the first and second input signals in conjunction with the rest of the limitation set forth in the claim.

The remaining claim, not specifically mentioned, is allowed because they are dependent upon one of the claim mentioned above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

*Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Emerson Puente, whose telephone number is (703) 305-8012. The examiner can normally be reached on Monday-Friday from 8:00AM- 5:00PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Robert Beausoliel*, can be reached on (703) 305-9713 or via e-mail addressed to *[robert.beausoliel@uspto.gov]*. The fax number for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to **[emerson.puente@uspto.gov]**.

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.




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Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 305-3900.

*Emerson Puente*

4/21/03

  
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